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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,815	07/21/2003	Marco Troost	P2001,0034	5766

24131 7590 04/14/2006

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,815	TROOST, MARCO	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1-3 and 5-13 are objected to because of the following informalities: The phrase "components/circuits/stages", as recited in claim 1, should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 1-3 and 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (5,455,453) in view of Chrysostomides et al. (5,646,434) and Shiga (5,416,660).

Harada et al. teach in figure 1 and related text a semiconductor component comprising: a semiconductor chip 8 including an electronic circuit configured therein, said electronic circuit having a terminal for a signal to be processed, said electronic circuit having a stage connected to said terminal for the signal, said electronic circuit having a terminal for obtaining a supply potential 3, said terminal for obtaining the supply potential being connected to said stage;

a first conductor track 9 running outside said semiconductor chip, said first conductor track being connected to said terminal for the signal;

a second conductor track 9 running outside said semiconductor chip, said second conductor track being connected to said terminal for obtaining the supply potential;

a further conductor track 4 running outside the entire components/circuits/stages of said semiconductor chip, said further conductor track being connected to said second conductor track, said further conductor track crossing said first conductor track, thus defining a crossing location and said further conductor track crossing said second conductor track.

Harada et al. do not teach a stage selected from a group consisting of an input stage and an output stage, and

an ESD protection element for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, said ESD protection element for carrying the electrostatic discharge disposed outside of said semiconductor chip; and said ESD protection element for carrying the electrostatic discharge connected outside of said semiconductor chip to said further conductor track and to said first conductor track.

Chrysostomides et al. teach in figures 1 and 5 and related text a stage selected from a group consisting of an input stage and an output stage, and an ESD protection element 13 for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, and said ESD protection element for carrying the electrostatic discharge connected outside of said semiconductor chip to said further conductor track and to said first conductor track.

Shiga teaches in figure 2a and related text an ESD protection element 2 for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, said ESD protection element for carrying the electrostatic discharge disposed outside of said semiconductor chip; and

said ESD protection element for carrying the electrostatic discharge connected outside of said semiconductor chip to said further conductor track and to said first conductor track.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a stage selected from a group consisting of an input stage and an output stage, and an ESD protection element for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, said ESD protection element for carrying the electrostatic discharge disposed outside of said semiconductor chip; wherein said ESD protection element for carrying the electrostatic discharge connected outside of said semiconductor chip to said further conductor track and to said first conductor track, in Harada et al.'s device, in order to use the device in an application which requires an ESD protection to an input and an output stage of the chip.

Regarding the claimed limitations of a ESD protection element being disposed close to said crossing location, these features are inherent in prior art's device because the ESD protection element is inherently disposed close to said crossing location.

Regarding claim 2, prior art teaches a package surrounding said semiconductor body and said further conductor track; said package partially surrounding said first conductor track such that a portion of said first conductor track facing toward said semiconductor chip runs inside said package and a portion of said first conductor track facing away from said semiconductor chip runs outside said package; and

said package partially surrounding said second conductor track such that a portion of said second conductor track facing toward said semiconductor chip runs inside said package and a portion of said second conductor track facing away from said semiconductor chip runs outside said package.

Regarding claim 3, prior art teaches said ESD protection element is a diode (Shiga); said diode has an anode connected to said further conductor track; and said diode has a cathode connected to said first conductor track.

Regarding claim 5, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an insulation material configured where said further conductor track crosses said first conductor track in Harada et al.'s device, in order to avoid short circuit the device.

Regarding claim 6, Harada et al. teach in figure 1 a third conductor track 9; a terminal for a signal and assigned to said third conductor track; and a further element (Chrysostomides et al. 13, 15) for carrying an electrostatic discharge; said further

conductor track running in a main direction and having a conductor track portion branching away from said main direction; said third conductor track crossing said further conductor track near said conductor track portion of said further conductor track; and said conductor track portion of said further conductor track is connected to said further element for carrying the electrostatic discharge.

Regarding claims 7-8, Harada et al. teach in figure 1 a bonding wire connecting said first conductor track to said terminal for the signal; and a bonding wire connecting said second conductor track to said terminal for obtaining the supply potential, wherein said terminal for the signal and said terminal for obtaining the supply potential are metallized areas configured in said semiconductor body.

Regarding claims 9 and 10, Chrysostomides et al. teach in figure 5 an input stage has at least one transistor with a gate connected to said terminal for the signal; said transistor has a drain terminal and a source terminal; said drain terminal or said source terminal of said transistor connected to said terminal for the supply potential.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an inverter as the input stage in Harada et al.'s device in order to use the device in an application which requires transistor and an inverter, respectively.

Regarding claim 11, Harada et al. teach in figure 1 and related text a package wall disposed outside said semiconductor chip and including said first conductor track, said first conductor track having a contact area connected to a terminal of said electrostatic discharge protection element, wherein the package wall comprising a lead frame.

Regarding claim 12, Harada et al. teach in figure 1 and related text said first conductor track is connected to said terminal for the signal through a bonding wire.

Claims 1-3 and 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. (6,476,486) in view of Chrysostomides et al. (5,646,434) and Shiga (5,416,660).

Humphrey et al. teach in figure 8 and related text a semiconductor component comprising: a semiconductor chip 20 including an electronic circuit configured therein, said electronic circuit having a terminal for a signal to be processed, said electronic circuit having a stage connected to said terminal for the signal, said electronic circuit having a terminal for obtaining a supply potential 3, said terminal for obtaining the supply potential being connected to said stage;

a first conductor track (any of the wires) running outside said semiconductor chip, said first conductor track being connected to said terminal for the signal;

a second conductor track (any of the wires) running outside said semiconductor chip, said second conductor track being connected to said terminal for obtaining the supply potential;

a further conductor track 15 running outside the entire components/circuits/stages of said semiconductor chip, said further conductor track being connected to said second conductor track, said further conductor track crossing said first conductor track, thus defining a crossing location and said further conductor track crossing said second conductor track;

a diode Z3 disposed outside of said semiconductor chip; and said diode connected outside of said semiconductor chip to said further conductor track and to said first conductor track.

Humphrey et al. do not teach a stage selected from a group consisting of an input stage and an output stage, and using the diode as an ESD protection element.

Chrysostomides et al. teach in figures 1 and 5 and related text a stage selected from a group consisting of an input stage and an output stage, and an ESD protection element 13 for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, and said ESD protection element for carrying the electrostatic discharge connected outside of said semiconductor chip to said further conductor track and to said first conductor track.

Shiga teaches in figure 2a and related text an ESD protection element 2 for carrying an electrostatic discharge away from said terminal for the signal and to the supply

potential, said ESD protection element for carrying the electrostatic discharge disposed outside of said semiconductor chip; and

said ESD protection element for carrying the electrostatic discharge connected outside of said semiconductor chip to said further conductor track and to said first conductor track.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a stage selected from a group consisting of an input stage and an output stage, and an ESD protection element for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, said ESD protection element for carrying the electrostatic discharge disposed outside of said semiconductor chip; wherein said ESD protection element for carrying the electrostatic discharge connected outside of said semiconductor chip to said further conductor track and to said first conductor track, in Humphrey et al.'s device, in order to use the device in an application which requires an ESD protection to an input and an output stage of the chip.

Regarding the claimed limitations of a ESD protection element being disposed close to said crossing location, these features are inherent in prior art's device because the ESD protection element is inherently disposed close to said crossing location.

Regarding claim 2, prior art teaches a package surrounding said semiconductor body and said further conductor track; said package partially surrounding said first conductor track such that a portion of said first conductor track facing toward said semiconductor

chip runs inside said package and a portion of said first conductor track facing away from said semiconductor chip runs outside said package; and

said package partially surrounding said second conductor track such that a portion of said second conductor track facing toward said semiconductor chip runs inside said package and a portion of said second conductor track facing away from said semiconductor chip runs outside said package.

Regarding claim 3, prior art teaches said ESD protection element is a diode (Shiga); said diode has an anode connected to said further conductor track; and said diode has a cathode connected to said first conductor track.

Regarding claim 5, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an insulation material configured where said further conductor track crosses said first conductor track in Humphrey et al.'s device, in order to avoid short circuit the device.

Regarding claim 6, Humphrey et al. teach in figure 8 a third conductor track 9; a terminal for a signal and assigned to said third conductor track; and a further element Z2 for carrying an electrostatic discharge; said further conductor track running in a main direction and having a conductor track portion branching away from said main direction; said third conductor track crossing said further conductor track near said conductor track portion of said further conductor track; and said conductor track portion of said

further conductor track is connected to said further element for carrying the electrostatic discharge.

Regarding claims 7-8, Humphrey et al. teach in figure 8 a bonding wire connecting said first conductor track to said terminal for the signal; and a bonding wire connecting said second conductor track to said terminal for obtaining the supply potential, wherein

said terminal for the signal and said terminal for obtaining the supply potential are metallized areas configured in said semiconductor body.

Regarding claims 9 and 10, Chrysostomides et al. teach in figure 5 an input stage has at least one transistor with a gate connected to said terminal for the signal; said transistor has a drain terminal and a source terminal; said drain terminal or said source terminal of said transistor connected to said terminal for the supply potential.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an inverter as the input stage in Humphrey et al.'s device in order to use the device in an application which requires transistor and an inverter, respectively.

Regarding claim 11, Humphrey et al. teach in figure 1 and related text a package wall disposed outside said semiconductor chip and including said first conductor track, said first conductor track having a contact area connected to a terminal of said electrostatic discharge protection element, wherein the package wall comprising a lead frame.

Regarding claim 12, Humphrey et al. teach in figure 1 and related text said first conductor track is connected to said terminal for the signal through a bonding wire.

Response to Arguments

Applicant's arguments with respect to claims 1-3 and 5-13 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
4/10/06

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